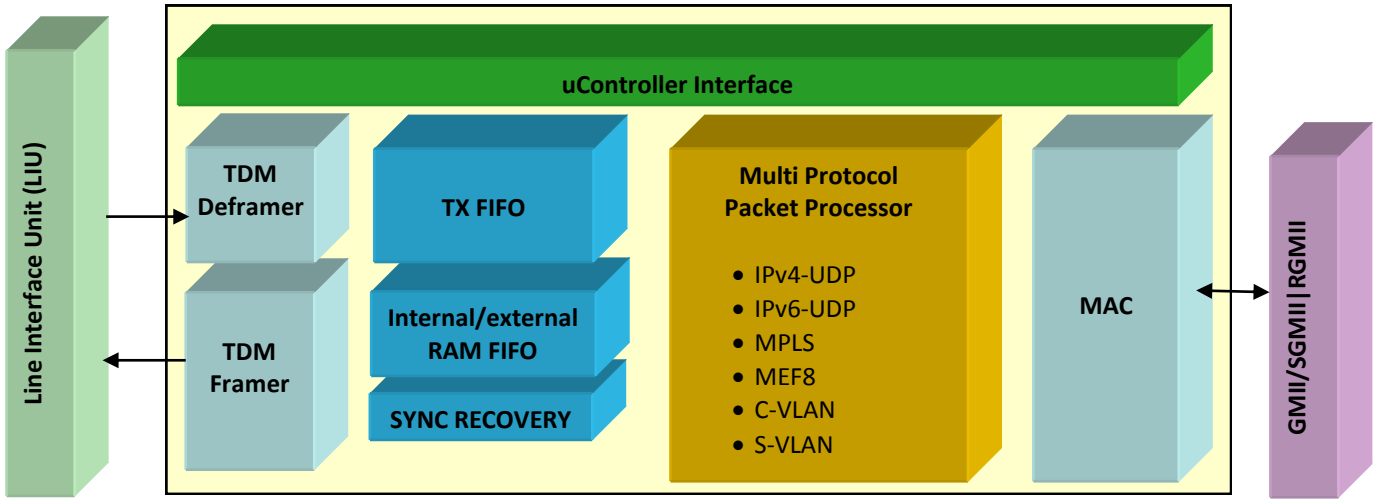
Inspiring partners for finding solutions

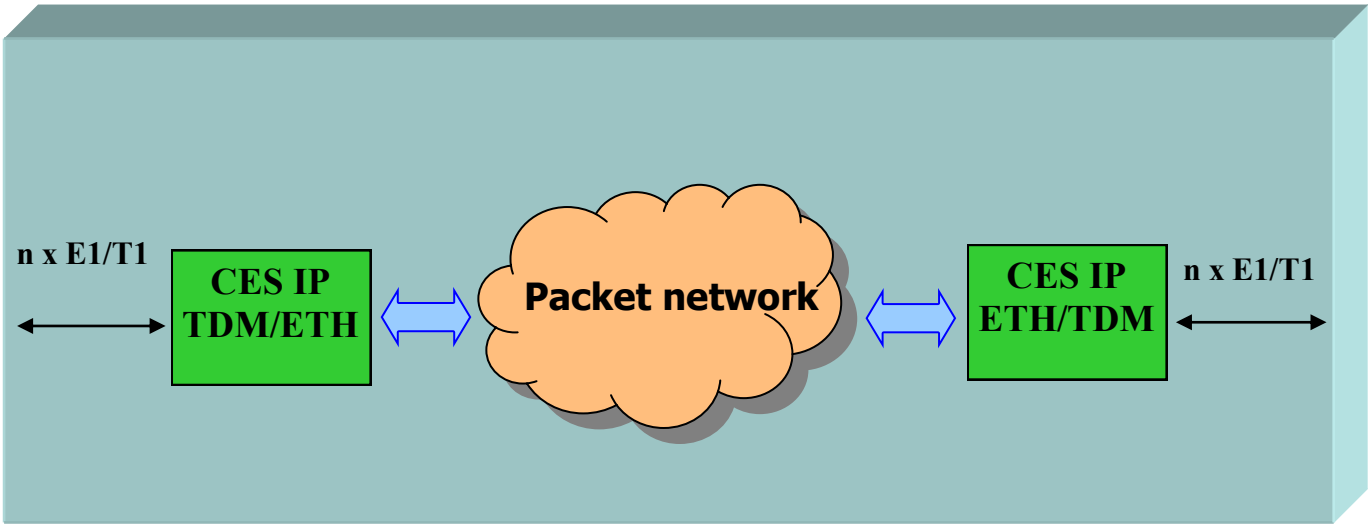
CES IP
First compliant with ITU-T G.8261

Where Ethernet and TDM meet



CES IP architecture

A full featured CESOP/SATOP-IP
Portable in any FPGA platform
Scalable and reliable (see G.8261 results)
Several packet protocols managed on ethernet side
SW control drivers provided
Customized solutions possible and demo board available



Overview

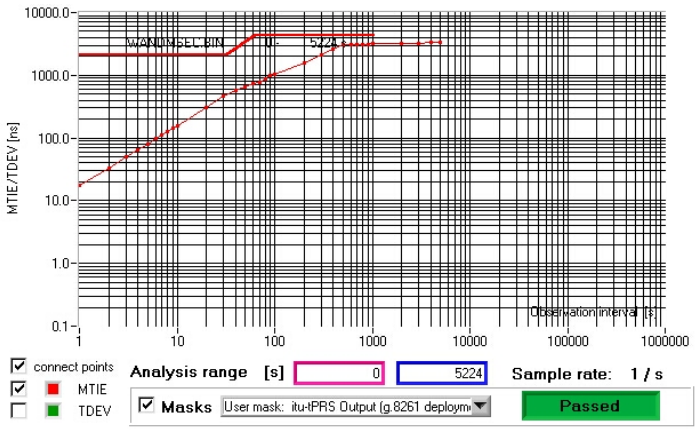
The CES IP (Circuit Emulation Service IP) developed by BTP Research provides the agnostic/structured emulation of a TDM E1/T1 service over Ethernet packets.
Complies with ITU-T recommendation Y.1413.
Complies with IETF standards CESoP and SAToP: RFC 4553 and RFC 5086.
Complies with MEF8 standard.
Complies also with ITU-T G.8261 (see diagrams on next pages).
The CES IP is capable of assembling user-defined packets of E1/T1 traffic from the TDM interface (external Line Interface Unit) and transmitting them out the packet interfaces using a variety of protocols and VLAN tagging.
The IP is able to manage up to 256 TDM channels.
It implements 3 different algorithms to recovery the TDM synchronization: adaptive, differential and synchronous. Also loop timing is provided.
Programmable packet delay variation is supported.
The TDM data stream will be arranged into Ethernet Packets which will be transmitted to an external Ethernet entity (e.g a L2 Switch) through a SGMII interface, but also alternative interface could be provided (GMII, RGMII ...).
A microprocessor interface will be also available to access the IP registers.
FPGA family: Altera, Xilinx, Lattice and Microsemi can support the IP according to channels numbers.

Features

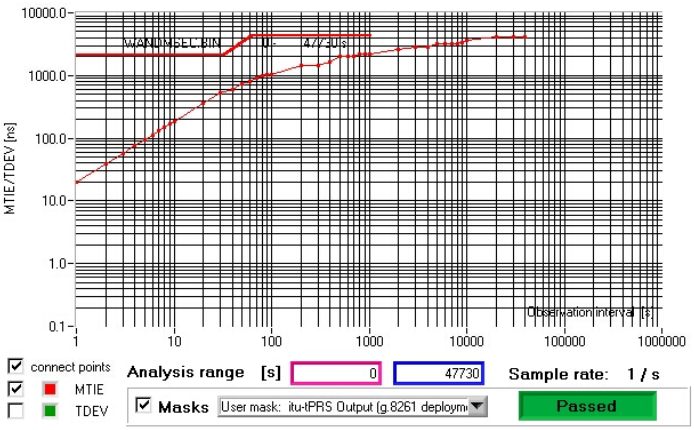
- TDM E1 signals compliant with ITU-T G.704 Framed with/without CRC4.
- TDM T1 signals compliant with GR-499 - Framed SF/ESF.
- Scalable number of channels up to 256 TDM channels.
- T1/E1 AIS detection, T1 Frame Aligner SF/ESF, E1 frame aligner with/without CRC4.
- AIS, RAI, Frame, CRC4, CRC6 alarms.
- TDM counters (CRC, LOF, LOM).
- Flexible different protocol packet encapsulation, on pseudo-wire based: IPv4-UDP, IPv6-UDP, MPLS, MEF8, C-VLAN, S-VLAN.
- Packet reordering.
- Packet Classifier.
- Support up to 256 different pseudo-wire connection across PSN.
- Adaptive/differential/synchronous/loop timing clock recovery.
- Structured Agnostic TDM circuit emulation.
- Structured Aware TDM circuit emulation.
- Grooming: 64Kbit switching function.
- Timestamp reordering.
- Programmable packet payload size from 64 to 1500 bytes.
- Auto-Centering.
- MAC Alarm and Counters (CRC32, MAC transmit and received packet).
- PWE3 alarms and counters.
- Up to 64 ms of Packet Delay Variation.
- TDM Loopback (near and far).
- Ethernet Loopback (near and far).
- Interface GMII/SGMII 1 Gbit/s.

Results of G.8261 test cases on CES IP

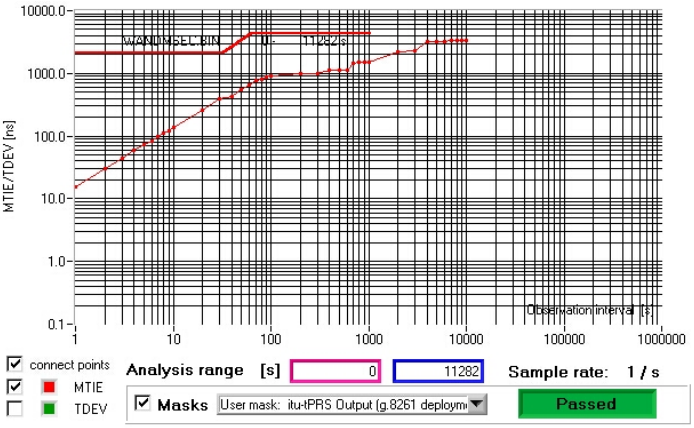
The following diagrams shows examples of results of test cases described in recommendation G.8261. All the resulting curves are in compliance with the masks reported in this recommendation. Tests have been performed on CES IP for E1 TDM traffic using ANUE Network Emulator. All others tests are available.



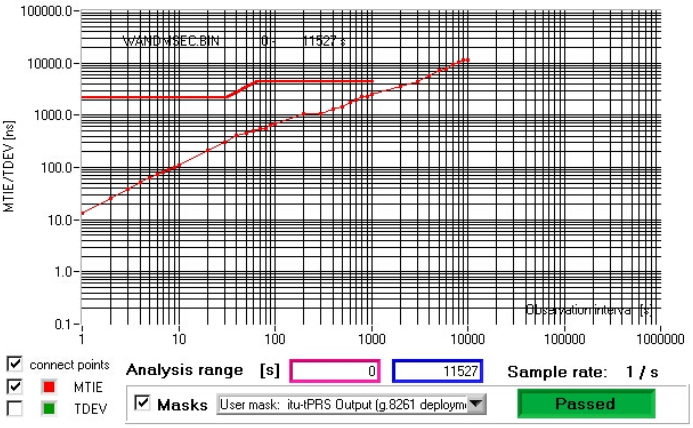
Test case 1: traffic model 2 MTIE



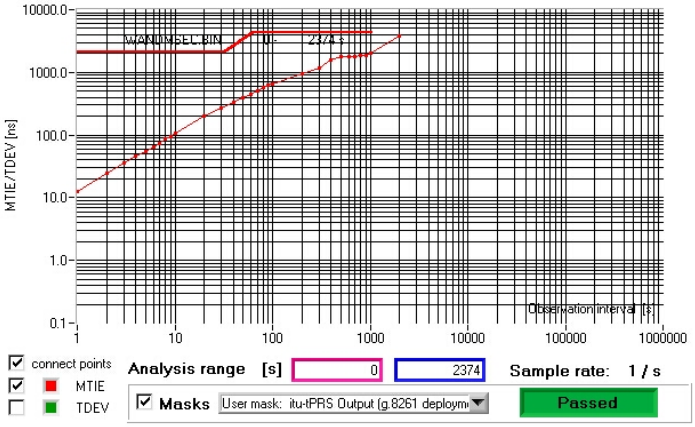
Test case 2: traffic model 2 MTIE



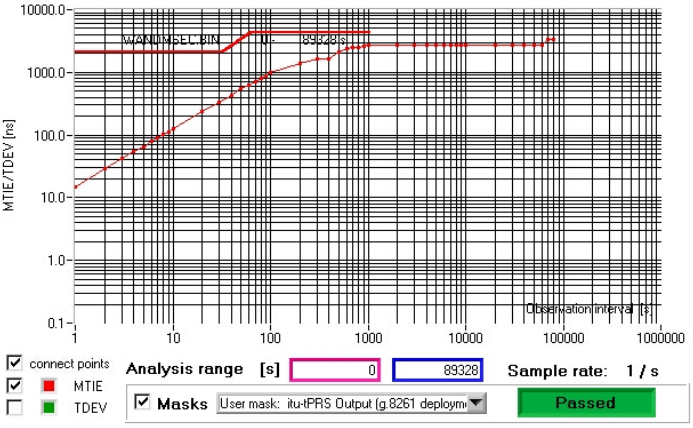
Test case 4: traffic model 2, 100 sec, drop MTIE



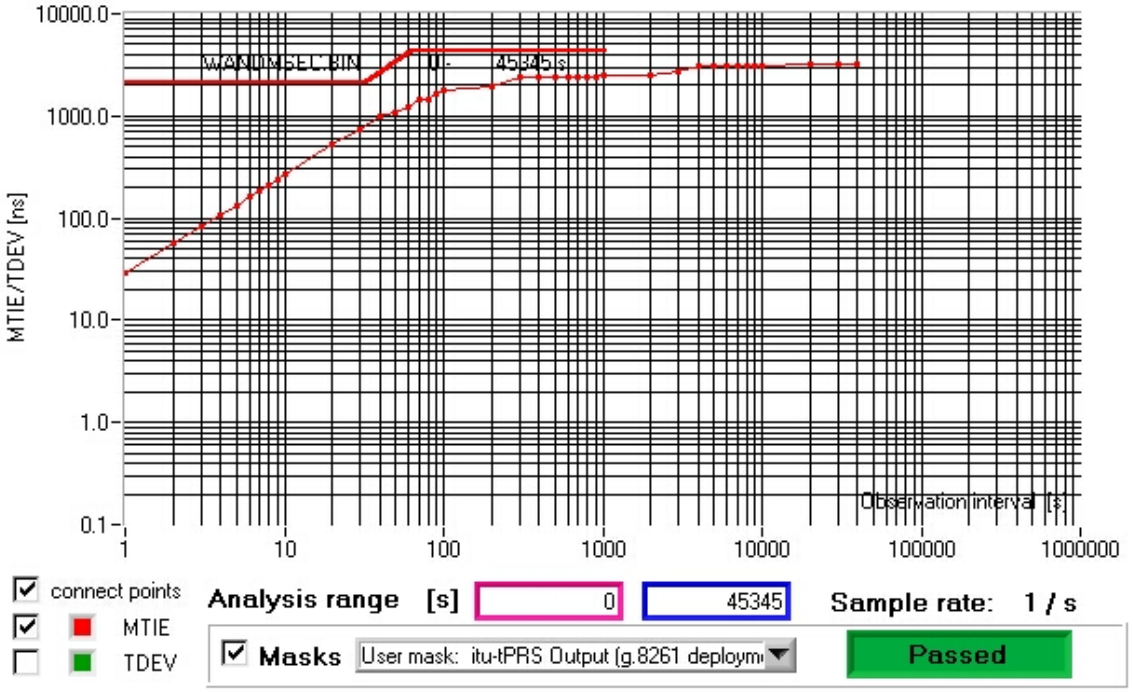
Test case 5: traffic model 2, 100 sec, drop MTIE



Test case 6: traffic model 2, bypass 1, 500 ms, drop MTIE



Test case 7: traffic model 2, 16 ppb MTIE



Test case 8b: MTIE

Protocols on Ethernet

Several protocols are configurable on Ethernet side:

- MEF8
- IPV4-UDP
- IPV6-UDP
- MPLS
- IPV4 over MPLS
- IPV6 over MPLS

All single fields are programmable.

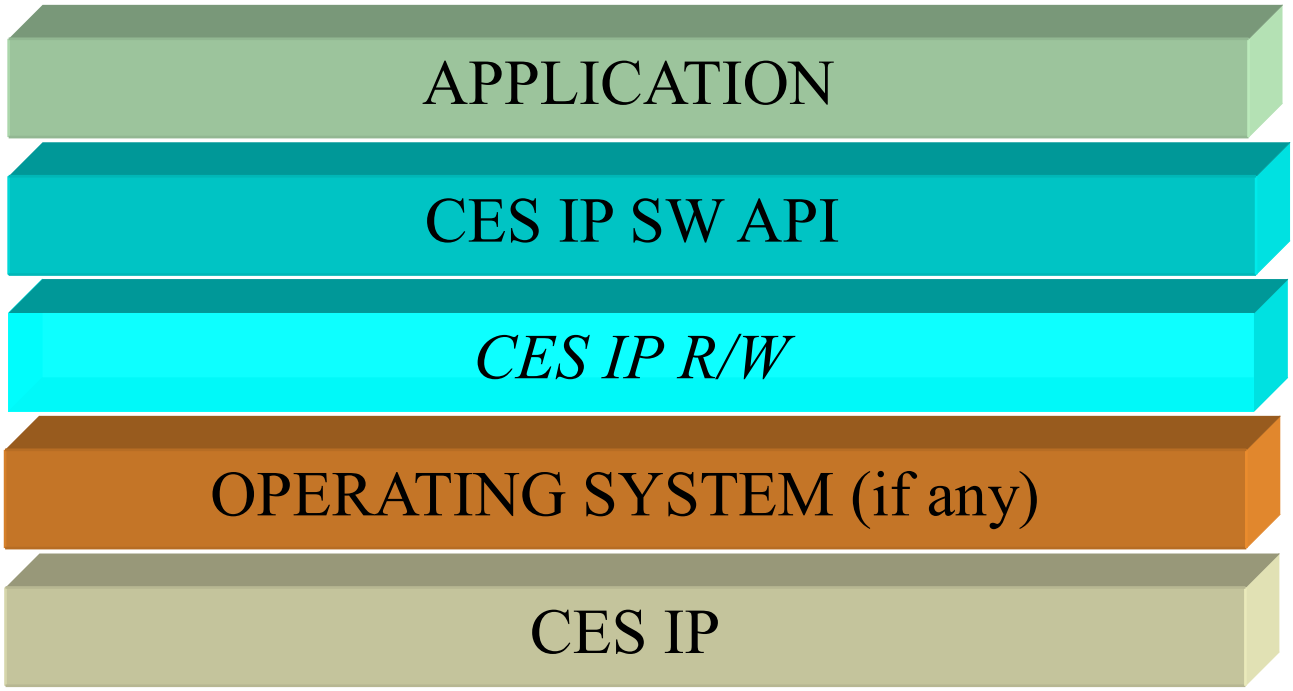
Single or double VLAN tagging can also be configured.

The structure of an IPV4-UDP packet (without RTP header) is shown in the diagram.

Bytes	Bits 0	1	2	3	4	5	6	7
1	Destination MAC Address [0:48]							
2								
3								
4								
5								
6								
7	Source MAC Address [0:48]							
8								
9								
10								
11								
12								
13	**EtherType IPV4 = 0x0800**							
14								
15	IPV4 Version = **0x04**				**IP Header Length = 5**			
16	DS & ECN (previous TOS)							
17	IP Total Length							
18								
19	Identification							
20								
21	Flags							
22	Fragment offset							
23	Time to live							
24	**Protocol = 0x11 (UDP)**							
25	IP Header Checksum							
26								
27	IP Source Address							
28								
29								
30								
31	IP Destination Address							
32								
33								
34								
35	UDP Source Port							
36								
37	UDP Destination Port (used for PWE3 function)							
38								
39	UDP Length							
40								
41	UDP Checksum							
42								
43	0	0	0	0	L	R	M[0:1]/RSV	
44	FRG		LEN					
45	CES Sequence Number [0:15]							
46								
47	*Octet 1*							
48	*Octet 2*							
	...							
	...							
	...							
	...							
	...							
	Octet nnn							
	Ethernet FCS [0:31]							

CES IP SOFTWARE INTERFACE

For the configuration of the CES IP it is available a SW Application Program Interface (API) written in C programming language and easily portable in any operating system (or even in a “bare metal” firmware) by only implementing READ/WRITE functions on CES IP.



BTP Research provides customers its experience and skills in electronic design related to many industrial fields: ranging from several existing variants of telecom applications, including the Defence industry, to many other branches of the electronic industry as Automotive, Biomedic and Automation. The BTP Research team has more than twenty years of experience in electronic design both for Hardware (PBA and FPGA/Asic) and Software/Firmware. Project management, cost analysis and Quality control are constantly applied during the development process. System level background expertise, as well as manufacturing knowledge, are now available to customers or partners who are looking for consolidated know how, experience and commitment to achieve the target .

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